

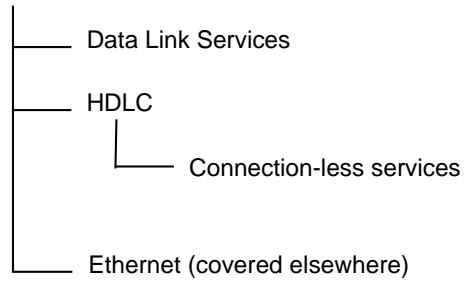
Functions of a Data Link Protocol

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- Framing PDUs
- Addressing Destination
- Error Detection / Error Recovery
- Link Management

Data Link Protocols

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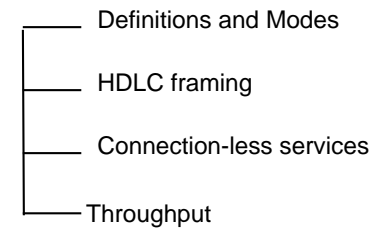


Components of a DL

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- Hardware
- Frame Format
- Protocol
- Buffer Memory
- Event Timers

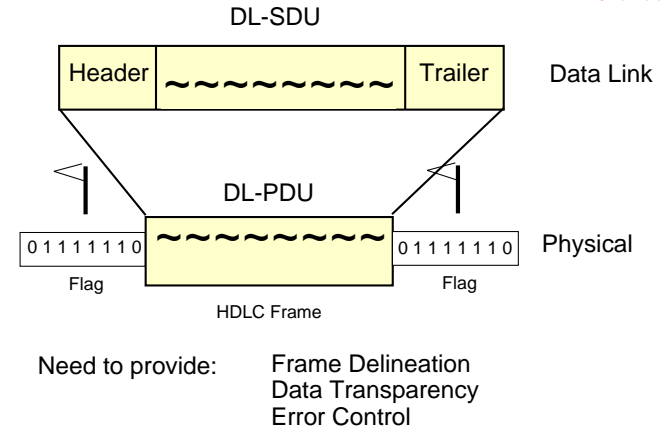
High Level Data Link Control Protocol



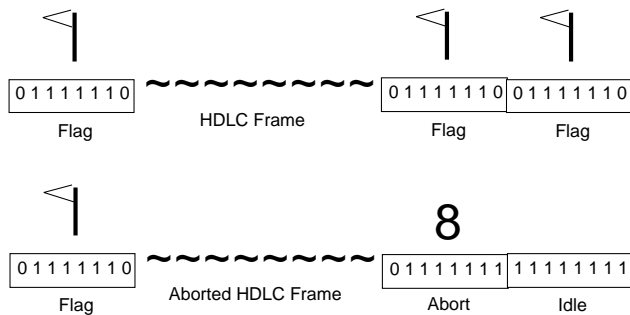
HDLC Framing

- Flags
- 0-bit insertion
- Cyclic Redundancy Check

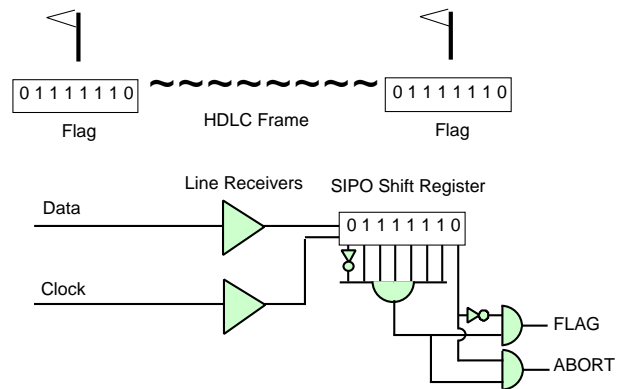
HDLC DATA LINK



HDLC Frame Delineation



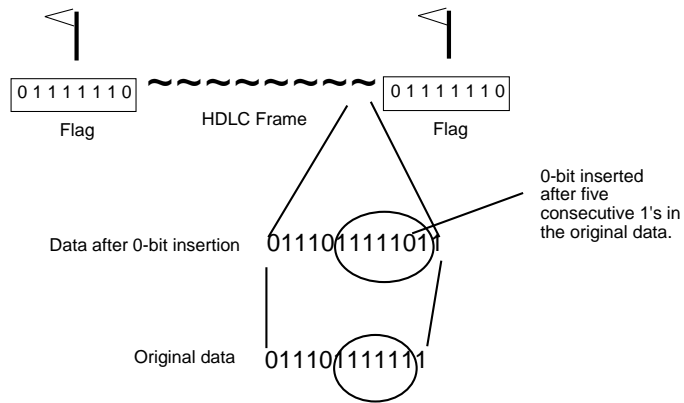
HDLC Flag Detection



N.B. Real implementation uses a Finite State Machine (FSM)

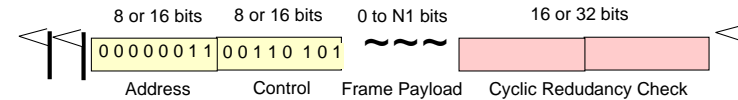
HDLC 0-Bit Insertion

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HDLC Frame Structure

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N1 = maximum number of bytes in the frame payload
 Typical values: 128 B, 576 B, 1500B, etc

HDLC CRC

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Why is a CRC needed?

To verify correctness of data
 What happens if we don't check?

How can data become corrupted?

Noise
 Interference
 Errors in network components
 Faulty cabling
 Cosmic rays ???

CRC Generator Polynomials

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$$\begin{aligned} \text{CRC-16} &= x^{16} + x^{12} + x^5 + x \\ \text{CRC-CCITT} &= x^{16} + x^{12} + x^5 + 1 \\ \text{CRC-32} &= x^{32} + x^{26} + x^{16} + \\ & \quad x^{12} + x^{11} + x^{10} + \\ & \quad x^5 + x^4 + x^2 + x + 1 \end{aligned}$$

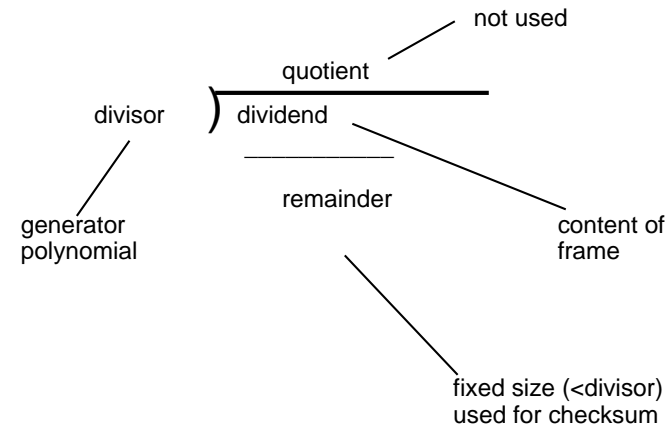
Cyclical Redundancy Check

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Properties of a CRC-16	Synchronous Block/Frame Protocols Implemented in Hardware
1-bit error	100% Detected
2-bit errors	100% Detected
Odd errors	100% Detected
Burst errors < 16 bits	100% Detected
Burst errors exactly 17 bits	99.9969% Detected
All other error bursts	99.9984 % Detected

Cyclical Redundancy Check

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CRC - Why Modulo 2 Division?

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Because the hardware solution is simple!!!!

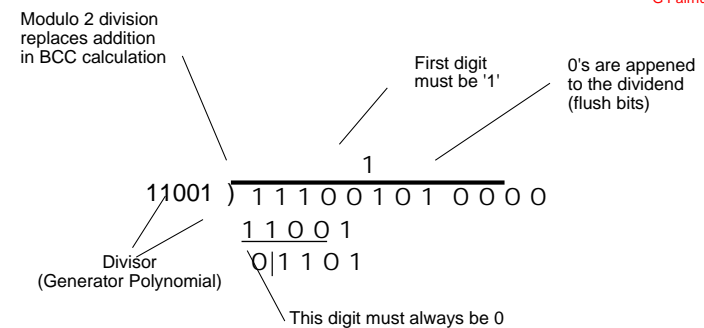
Truth Table for Modulo-2 Division (XOR)

0	0 = 0
0	1 = 1
1	0 = 1
1	1 = 0

CRC calculations ignore the carry

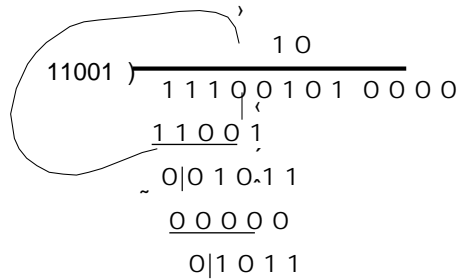
CRC Example (1)

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CRC Example (2)

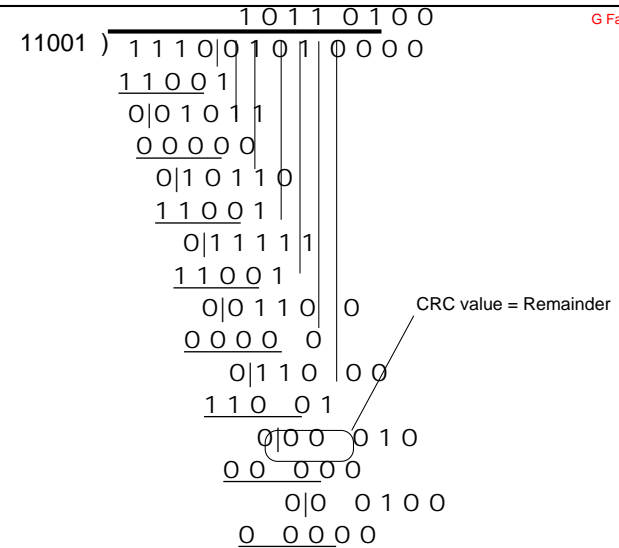
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- < Bring next digit of dividend down
- > Copy msb of value to quotient
- ^ Insert 0 (if quotient 0) or divisor (if quotient 1)
- ^ Calculate XOR sum
- ~ Discard msb of value (always 0)

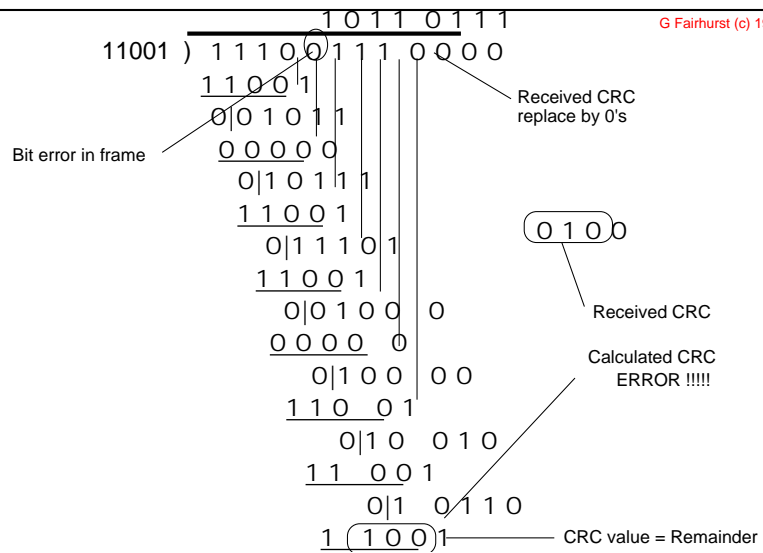
CRC Example (3)

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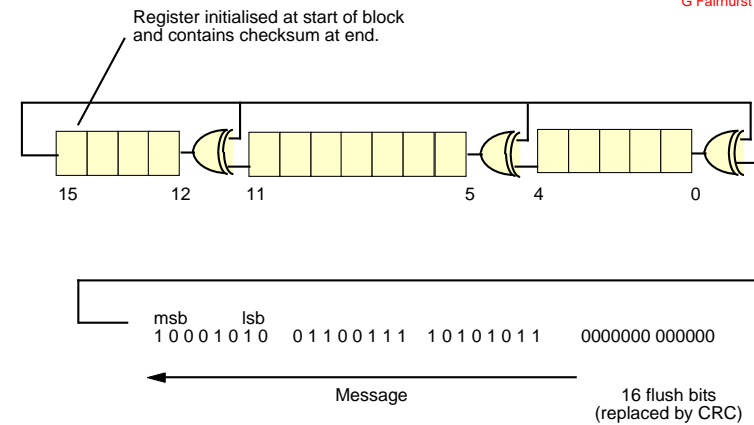
CRC Example (4)

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CRC Hardware

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HDLC Frame Layer Summary

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Synchronous Transmission

Clock and Data required at the receiver

Bit-Oriented Protocol (Transparent)

Frames delimited by flags

Hardware support required

Any data may be sent in payload

Transmitted frame size depends upon payload

Integrity checked by a CRC

Frames with good CRC forwarded

Frames with error CRC discarded

Frames terminated by abort sequence also discarded

3 Architectures

Multi-drop bus

Point to Point link \

Token passing ring <--- **This is covered by the course**

What you should know!

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You should know....

HDLC is a standard for synchronous communications

HDLC is bit-oriented

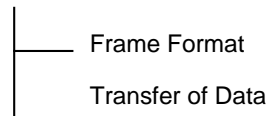
HDLC uses a cyclic redundancy checksum

HDLC supports 3 architectures

Best Effort Service

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HDLC Connection-Less Service



A best effort service

provides no guarantee of delivery

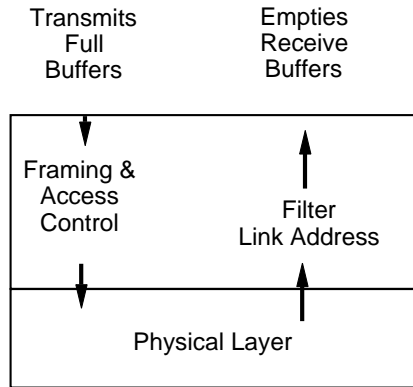
provides no notification of loss

provides no protection from duplication

provides no guarantee of original order

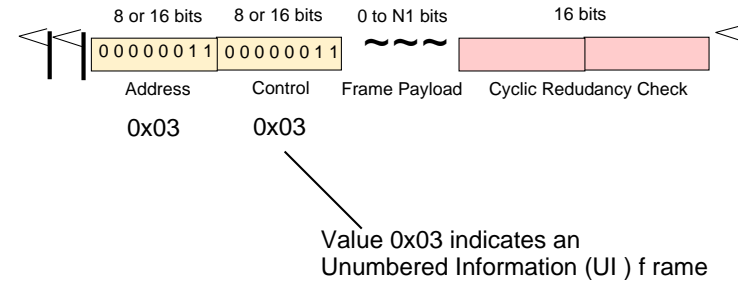
Basic Connection-Less Service

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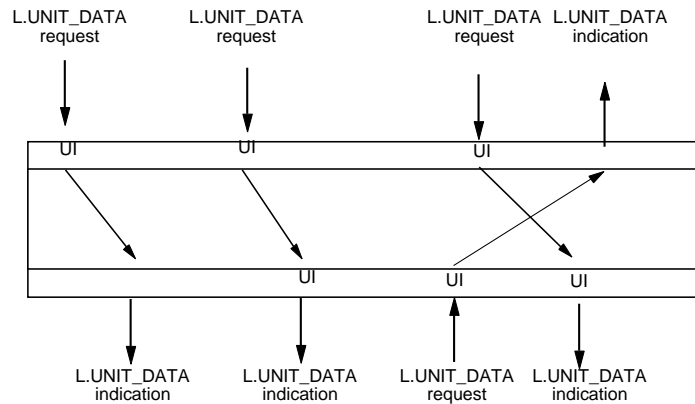
UI Frame Format

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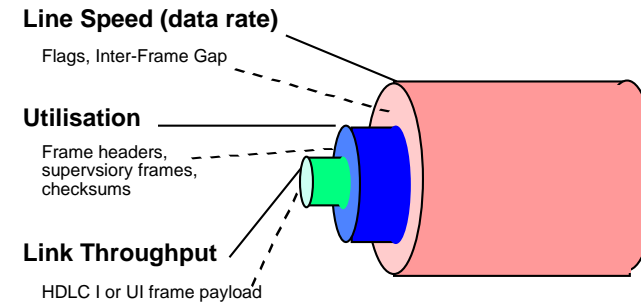
HDLC Connectionless Service

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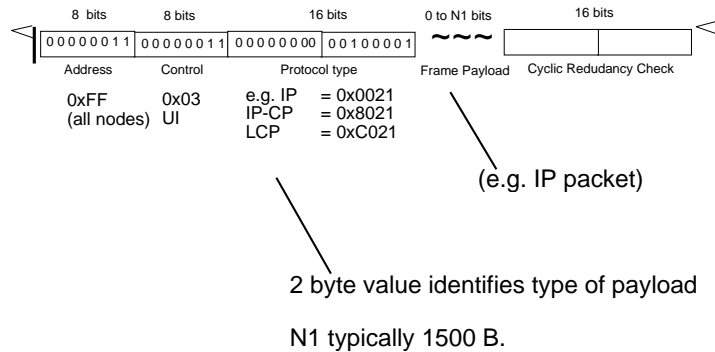
HDLC Performance

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Point-to-Point Protocol (PPP)

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RFC 1134, 1989

Reliability

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Implies....

- All information is received (no loss, no residual errors)
- No information is duplicated (no extra copies)
- Sequencing (original order is preserved)

Self - Help THINGS TO THINK ABOUT (1)

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Do you know:

How the data link receiver finds the start of:

- (a) An Ethernet Frame
- (b) An HDLC Frame

How the receiver finds the end of:

- (a) An Ethernet Frame
- (b) An HDLC Frame

??

What is a Best Effort Service?

Reliability

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Connection-Less	Connection-Oriented
Best Effort	Reliable
CRC Required	CRC Required
Simple Parameter Negotiation	Link Management
No Confirmed Delivery	Acknowledgments
No Flow Control (?)	Flow Control
No Error Control	ARQ